AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A raster engine for interfacing a frame buffer in a computer system to one of a plurality of disparate displays, comprising:

at least one control register programmable via the computer system to select a display mode;

a dual port RAM device operative to obtain pixel data from the frame buffer; and

a logic device having a parallel output, the logic device being adapted to select appropriate pixel data from the dual port RAM device according to the selected display mode, and to remap the selected pixel data according to the selected display mode;

the raster engine provides the remapped selected pixel data at the parallel output via the logic device according to a universal routing scheme applicable to the plurality of disparate displays.

2. (Original) The raster engine of claim 1, wherein the selected display mode comprises one of single pixel per clock up to 24 bits wide, single 16 bit 565 pixel per clock, single 16 bit 555 pixel per clock, single 24 bit pixel on 18 lines, single 16 bit 565 pixel on 18 lines, single 16 bit 555 pixel on 18 lines, 2 pixels per clock, 4 pixels per clock, 8 pixels per shift clock, 2 2/3 pixels per clock, and dual 2 2/3 pixels per clock.

3. (Original) The raster engine of claim 2, further comprising one of a look up table, a grayscale generator, and a blink logic system, wherein the logic device receives the selected pixel data from the dual port RAM device via the one of the look up table, the grayscale generator, and the blink logic system according to the selected display mode.

4. (Original) The raster engine of claim 3, wherein the logic device comprises a multiplexer.

5. (Original) The raster engine of claim 1, wherein the logic device is adapted to provide the selected pixel data to the output device in a 24 bit parallel format when the selected display mode is one of single 16 bit 565 pixel per clock and single 16 bit 555 pixel per clock.

6. (Original) The raster engine of claim 5, wherein the logic device is further adapted to copy a plurality of most significant bits from the selected pixel data into a corresponding plurality of unused least significant bits in the 24 bit parallel format, whereby improved color intensity range is provided.

7. (Original) The raster engine of claim 6, further comprising one of a look up table, a grayscale generator, and a blink logic system, wherein the logic device receives the selected pixel data from the dual port RAM device via the one of the look up table, the grayscale generator, and the blink logic system.

8. (Original) The raster engine of claim 7, wherein the logic device comprises a multiplexer.

9. (Original) The raster engine of claim 1, further comprising one of a look up table, a grayscale generator, and a blink logic system, wherein the logic device receives the selected pixel data from the dual port RAM device via the one of the look up table, the grayscale generator, and the blink logic system.

10. (Original) The raster engine of claim 1, wherein the selected display mode comprises a color mode, a shift mode, and a pixel mode.

11. (Original) The raster engine of claim 10, wherein the color mode comprises one of a look up table mode, triple 8 bits per channel, 16 bit 565 color mode, 16 bit 555 color mode, and a grayscale palette enabled mode.

12. (Original) The raster engine of claim 11, wherein the shift mode comprises one of single pixel per pixel clock up to 24 bits wide, single 24 bit or 16 bit pixel mapped to 18 bits per pixel clock, 2 pixels per shift clock up to 9 bits wide, 4 pixels per shift clock up to 4 bits wide, 8 pixels per shift clock up to 2 bits wide, 2 2/3 pixels per clock over 8 bit bus 3 bits wide, and dual 2 2/3 pixels per clock over dual 8 bit busses 3 bits wide.

13. (Original) The raster engine of claim 12, wherein the pixel mode comprises one of 4 bits per pixel, 8 bits per pixel, 16 bits per pixel, 24 bits per pixel, and 32 bits per pixel.

14. (Original) The raster engine of claim 11, wherein the pixel mode comprises one of 4 bits per pixel, 8 bits per pixel, 16 bits per pixel, 24 bits per pixel, and 32 bits per pixel.

15. (Original) The raster engine of claim 10, wherein the pixel mode comprises one of 4 bits per pixel, 8 bits per pixel, 16 bits per pixel, 24 bits per pixel, and 32 bits per pixel.

16. (Original) The raster engine of claim 15, wherein the shift mode comprises one of single pixel per pixel clock up to 24 bits wide, single 24 bit or 16 bit pixel mapped to 18 bits per pixel clock, 2 pixels per shift clock up to 9 bits wide, 4 pixels per shift clock up to 4 bits wide, 8 pixels per shift clock up to 2 bits wide, 2 2/3 pixels per clock over 8 bit bus 3 bits wide, and dual 2 2/3 pixels per clock over dual 8 bit busses 3 bits wide.

17. (Original) The raster engine of claim 10, wherein the shift mode comprises one of single pixel per pixel clock up to 24 bits wide, single 24 bit or 16 bit pixel mapped to 18 bits per pixel clock, 2 pixels per shift clock up to 9 bits wide, 4 pixels per shift clock up to 4 bits wide, 8 pixels per shift clock up to 2 bits wide, 2 2/3 pixels per clock over 8 bit bus 3 bits wide, and dual 2 2/3 pixels per clock over dual 8 bit busses 3 bits wide.

18. (Original) The raster engine of claim 13, wherein the logic device comprises a multiplexer.

19. (Original) The raster engine of claim 1, wherein the logic device comprises a multiplexer.

20. (Original) The raster engine of claim 1, wherein the selected display mode comprises a direct display command interface.

21-33. (Cancelled).